Remarks

Claims 1-11, 15-17 and 41-68 are pending. Claims 1-4, 6, 8-11, 15-16, 41-44, 46, 48-53, 55-58, 60 and 62-67 are amended to correct typographical and grammatical errors. These amendments present these claims in better form for consideration on appeal. As such amendments are authorized under 37 C.F.R. § 1.116(b)(2), Applicants therefore respectfully request their entry.

The Examiner rejected Claims 1-11, 15-17 and 41-54 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,427,968 (the "Hong '968 Patent") in view of U.S. Patent 6,018,178 ("Sung"). With respect to independent Claims 1 and 41, the Examiner states, in pertinent parts:

> With respect to claim 1, Hong teaches an electrically alterable memory device substantially as claimed including:
>
> * * *
>
> a first floating gate (60) having a first height and comprised of a conductive material, the first floating gate (60) disposed adjacent the first diffusion region (62) and above the first channel region and separated therefrom by a first insulator region (58), the first floating gate capable of storing electrical charge;
>
> a second floating gate (60) having a second height and comprised of a conductive material, the second floating gate (60) disposed adjacent the second diffusion region (62) and above the first channel region and separated therefrom by a second insulator region (58), the second floating gate (60) capable of storing electrical charge; and
>
> * * *
>
> Thus, Hong is shown to teach all the features of the claim with the exception of explicitly disclosing a first semiconductor layer doped with a first dopant located under the second semiconductor layer.
>
> * * *

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> Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the electrically alterable memory device of Hong on the semiconductor substrate having first and second semiconductor layer as taught by Sung to isolate the devices of different characteristics from each other.
>
> With respect to claim 41, Hong teaches an electrically alterable memory device substantially as claimed including:
>
> * * *
>
> a first floating gate (60) having a left side and a right side and comprising of a conductive material, the first floating gate (60) disposed adjacent the first diffusion region (62) and above the first channel region and separated therefrom by a first insulator region (58), the first floating gate (62) capable of storing electrical charge;
>
> a second floating gate (60) having a left side and a right side and comprising of a conductive material, the second floating gate (60) disposed adjacent the second diffusion region (62) and above the first channel region and separated therefrom by a second insulator region (58), the second floating gate (60) capable of storing electrical charge; and
>
> * * *
>
> Thus, Hong is shown to teach all the features of the claim with the exception of explicitly disclosing a first semiconductor layer doped with a first dopant located under the second semiconductor layer.
>
> * * *
>
> Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the electrically alterable memory device of Hong on the semiconductor substrate having first and second semiconductor layer as taught by Sung to isolate the devices of different characteristics from each other.

Applicants respectfully submit that the Examiner's rejection is invalid because the Examiner's reading of the Hong '968 patent requires a modification that would render the Hong '968 Patent unsatisfactory for its intended purpose (MPEP § 2143.01(V)). Contrary to the Examiner's assertions above, the Hong '968 Patent neither discloses nor suggests the first

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and second floating gates recited in each of Applicants' Claims 1 and 41. Instead, as explained in col. 4, lines 20-29 of the Hong '968 Patent, gate structure 60 -- which the Examiner relies upon for teaching both the first and the second floating gates -- is a single ring-shape floating gate:

> Referring again to FIGS. 3, 4d and 5d, as can be seen clearly, the memory cell configuration as fabricated in accordance with the described process steps has a special floating-gate structure 60. Both its shape and process steps of construction are similar to that of a conventional spacer oxide layer, but here, instead of being a simple oxide layer, it forms a polysilicon gate structure. The gate structure 60 surrounds the channel region and thus takes an annular or ring shape.

The Hong '968 Patent relies on this single ring-shaped floating gate 60 to solve a problem the Hong '968 Patent considers significant – i.e., increasing the number of possible program/erase cycles. The Hong '968 Patent explains the role of ring-shaped floating gate 60 in solving this problem in its specification, at col. 4, lines 44-62:

> [T]he memory cell configuration of the present invention, as shown in FIGS. 4d and 5d, is also freed of the severe limitation on the number of permitted program/erase cycles found in tile prior art split-gate configuration (such as the device of FIGS. 2a and 2b,) which relies on the single-sided program and erase operation from the drain region. More particularly, referring again to FIG. 6, the memory cell configuration of the present invention can utilize the drain region 62 (D) to inject electrons into the ring-shaped floating gate 60 via the tunneling oxide layer that is close to the drain region 62 (D) to facilitate the programming operation. When erasure is required, the source region 62 (S) can be utilized to expel electrons from the ring-shaped floating gate 60 via the tunneling oxide layer that is close to the source region 62 (S) to facilitate the erasure operation. Due to the configuration of separated tunneling regions, the number of possible program/erase cycles for a particular memory cell is greatly increased.
>
> (emphasis added)

Implicit in the Examiner's reading of single ring-shaped floating gate 60 of the Hong

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'968 Patent on the first and the second floating gates of each of Applicants' Claims 1 and 41 is the severing of single ring-shaped floating gate 60 into two separate floating gates. Such a modification would render inoperable the function of the single ring-shaped floating gate 60 (i.e., injecting electrons during programming at drain 62D and expelling electrons during erasure at source 62S), as taught by the Hong '968 Patent in the above-quoted portion of its Specification. MPEP § 2143.01 states that such a modification mandates the conclusion that the Hong '968 Patent neither suggests nor motivates the Examiner's modification:

> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)

Accordingly, Applicants respectfully submit that Claims 1 and 41, and their respective dependent Claims 2-11, 15-17 and 42-54 are each allowable over the combined teachings of the Hong '968 Patent and Sung. Reconsideration and allowance of Claims 1-11, 15-17 and 41-54 are therefore requested.

The Examiner rejected Claims 55-68 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,576,232 (the "Hong '232 Patent") in view of Sung. With respect to Claim 55, the Examiner states, in pertinent parts:

> With respect to claim 55, Hong teaches an electrically alterable memory device substantially as claimed including:
>
> * * *
>
> a first floating gate (580) having a first height and comprised of a conductive material, the first floating gate (580) disposed adjacent the first diffusion region (59) and above the first channel region and separated therefrom by a first insulator region (57), the first floating gate (580) capable of storing electrical charge;
>
> a second floating gate (580) having a second height and

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> comprised of a conductive material, the second floating gate (580) disposed adjacent the second diffusion region (59) and above the first channel region and separated therefrom by a second insulator region (57), the second floating gate (580) capable of storing electrical charge; and
>
> * * *
>
> Thus, Hong is shown to teach all the features of the claim with the exception of explicitly disclosing a first semiconductor layer doped with a first dopant located under the second semiconductor layer.
>
> * * *
>
> Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the electrically alterable memory device of Hong on the semiconductor substrate having first and second semiconductor layer as taught by Sung to isolate the devices of different characteristics from each other.

Applicants respectfully traverse the Examiner's rejection. As in the specification of the Hong '968 Patent, the specification of the Hong '232 Patent neither discloses nor suggests the first and second floating gates recited in Applicants' Claim 55. As explained in col. 5, lines 3-11 of the Hong '232 Patent, the sidewall spacers 580 -- which the Examiner relies upon for teaching both the first and the second floating gates -- is a single floating gate, the two spacers being electrically connected together by conductive strips 540:

> Each of sidewall spacers 580, being a conductor itself also cover the area of tunnel oxide layer 57 near the generally vertical sidewall of isolating oxide layers 570, as well as the exposed edges of gate dielectric layer 53, while being isolated from control gate 520. Conducting strips 540 and sidewall spacers 580, being directly and electric-conductingly connected to each other, together constitute the floating gate of the memory cells of the flash memory device.
>
> (emphasis added)

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As in the case of ring-shaped floating gate 60 of the Hong '968 Patent, implicit in the Examiner's reading of single floating gate formed by spacers 580 and conductive strips 540 of

the Hong '232 Patent on the first and the second floating gates of Claim55 is the severing of the single floating gate (580-540) into two separate floating gates. Such a modification would destroy the function of the single floating gate in providing precise channel length control, as taught by the Hong '232 Patent, at col. 5, lines 26-41:

> This split-gate flash memory device has a total channel length L, which includes one isolation transistor channel length L_1 and two floating-gate transistor channel lengths L_2. Both lengths L_2 and L_2 are not controlled by the photolithography method as is used in the prior art process. Instead, floating gate channel length L_2 can be well-controlled by the thickness of sidewall spacers 580. As mentioned above, this precisely-aligned channel dimensioning is important for the correct and reliable operation of the memory cell. If a device is fabricated in accordance with the present invention, erasure and writing operations of the memory cells can be implemented and separated from both sides of the cell unit. This capability improves the endurance of the memory device in terms of the number of information erasures and programming conducted during the lifetime of the device.
>
> (emphasis added)

Thus, Applicants respectfully submit that Claim 55 and its dependent Claims 56-68 are each allowable over the combined teachings of the Hong '232 Patent and Sung, as there is no basis for the Examiner's proposed modification of the teachings of the Hong '232 Patent, as explained in MPEP § 2143.01(V). Reconsideration and allowance of Claims 55-68 are therefore requested.

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Therefore, for the reasons set forth above, all pending claims (i.e., Claims 1-11, 15-17 and 41-68) are allowable over the art of record. If the Examiner has any question regarding the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant at 408-392-9250.

Certificate of Transmission: I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. 571-273-8300 on August 14, 2006.

Attorney for Applicant(s) Date of Signature 8/14/2006

Respectfully submitted,

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